IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#13/Affidavit
Amarche
4/10/00

In r application of:

E. Colgan et al.

Serial No.: 08/999,663

Filed: December 18, 1997

Date: January 31, 2000

Group Art Unit: 2871

Examiner: J. Dudek

Docket No.: YO994-065XX

For: A REFLECTIVE SPATIAL LIGHT MODULATOR ARRAY

Assistant Commissioner for Patents
Washington, D.C. 20231

I hereby certify that this paper is being facsimile transmitted under Rule CFR 1.61(d) to the U.S. Patent and Trademark Office on the date shown above.

Daniel P. Morris
Reg. No. 32,053

FAX COPY RECEIVED
APR 05 2000
TECHNOLOGY CENTER 2800

AFFIDAVIT UNDER 37 CFR 1.131

We, Evan G. Colgan, James M.E. Harper and James L. Speidell declares as follows:

We are co-inventors of the invention of the subject matter of the above-identified patent application. As evidenced by the attached copy of our invention disclosure we conceived and reduced the invention to practice prior to October 3, 1993 the filing date of US patent 5,461,501 to Sato et al. The attached invention disclosure was signed by us and be two witnesses and bears a time stamp of the IBM Yorktown Intellectual property Law Department prior to October 3, 1993. All dates have been obliterated.

The undersigned affiant swears further that all statements made herein of his own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or patent issuing thereon.

By: Evan G. Colgan
Evan G. Colgan

State of New York)ss.:
County of Westchester)

On this 31st day of January, 2000, before me personally came Evan G. Colgan to me personally known, and known to me to be the person described in and who executed the foregoing assignment, and he acknowledged to me that he executed the same as his free act and deed.

Jennifer A. Smith
Notary

JENNIFER A. SMITH
Notary Public, State of New York
No. 01SM5063001
Qualified in Westchester County
Commission Expires July 15, 2000

By: James M.E. Harper
James M. E. Harper

State of New York)ss.:
County of Westchester)

On this 28th day of January, 2000, before me personally came James M. E. Harper to me personally known, and known to me to be the person described in and who executed the foregoing assignment, and he acknowledged to me that he executed the same as his free act and deed.

Jennifer A. Smith
Notary

JENNIFER A. SMITH
Notary Public, State of New York
No. 01SM5063001
Qualified in Westchester County
Commission Expires July 15, 2000

By: James L. Speidell
James L. Speidell

State of New York)ss.:
County of Westchester)

On this 1st day of February, 2000, before me personally came James L. Speidell to me personally known, and known to me to be the person described in and who executed the foregoing assignment, and he acknowledged to me that he executed the same as his free act and deed.

Jennifer A. Smith
Notary

JENNIFER A. SMITH
Notary Public, State of New York
No. 01SM5063001
Qualified in Westchester County
Commission Expires July 15, 2000

S.N. 08/999,6

IBM Confidential

Page 1 of 4

IBM Inventi n Disclosure

12-258

ULL NAME(S) OF INVENTOR(S)	USERID/NODE	EMP. SER.	DIV/DEPT	BLDG/ZIP	LOCATION	TEL. NUM.
un Colgan 331469	862-29/ YKTVMV 4774	In NP	RES/ 743	LGA/COLGA	Yorktown	945-2909
mes M. Harper 129 353	862-14 YKTVMV 4773	In YP	RES/ 742	ARP/HARPER	Yorktown	945-1663
ank Kaufman 550004	862-32/ YKTVMV 4120	In NP	RES/ 743	/FBK	Yorktown	945-3208
rgaret P. Manny 671700	862-12/ YKTVMV 4180	In YP	RES/ 748	/MANNY	Yorktown	945-1273
bert L. Melcher 763725	862-41/ YKTVMV 4203	In YP	RES/ 450	/MELCHER	Yorktown	945-4129
mes L. Speidell 592061	862-18/ YKTVMV 5001	In YP	RES/ 414	/SPEIDEL	Yorktown	945-1862

FOR USE BY IPLaw
DISCLOSURE NO. [redacted]
PATENT ATTY. RMT
EVALUATOR PAR
WHERE & WHEN RECEIVED (Time Stamp) [redacted]
IBM YORKTOWN

TLE OF INVENTION *(Short & Descriptive)*

Planarized Structure and Process for Reflective Light-Valve Array

ROBLEM SOLVED BY THIS INVENTION *(Summary)*

A planarized structure and process to fabricate'it are described. The structure begins with a silicon wafer on which CMOS circuits have been fabricated. The wafer is then planarized using a chem-mech polish. An optical barrier is fabricated to prevent light from interacting with the underlying CMOS circuits. A stud is fabricated to make electrical contact between the CMOS circuits and individual mirrors which are to be fabricated on the wafer electrically isolated from the optical barrier and each other. A spacer is fabricated to support the glass cover plate. A procedure is described for using a step and repeat lithographic tool to expose with geometric precision millions of individual mirrors over an area larger than the exposure field of the step and repeat tool.

CKGROUND INFORMATION

To what ☐IBM Project, ☐Proposal, ☐or Product, ☐or government contract is this invention related? Projection Display
Related and background publications: None cited
Keywords for database search for related work: Projection Display, Spatial Light Modulator, Light-Valve
Critical Dates:
Suggested Evaluator: DEPP HORN

VENTOR ON INTERNATIONAL ASSIGNMENT. Is any inventor of this disclosure in this country on assignment from another country?
☐YES, ☑NO. If "Yes", see instruction #5.

SCRIPTION OF INVENTION - *Provide a description (including sketches and diagrams as required). On systems disclosures list significant functions and show where each is accomplished. ... disclosures need show only a flowchart and describe what your invention does at the level of the invention.*

The Problem

Light-valve arrays are used in projection displays, optical interconnect, optical computing, and other applications in which light is to be directed in specific directions based on a prescribed function and/or pattern. (We use light-valve array and spatial light modulator synonymously). Four of the factors which affect the performance of the light-valve array are: (i) Optical through-put. This is enhanced by using a reflective array with high aperture ratio and highly reflecting mirrors. High aperture ratio demands that the mirrors are individually large compared to the gaps between them: this requires precise fabrication. High reflectivity requires using a highly reflective metal such as Al or Ag, and fabricating it on a smooth and flat surface. (ii) Light must be kept from interacting with the underlying CMOS circuits; thus an optical barrier must be fabricated preventing the incident light from reaching the CMOS circuits. (iii) If used in the normally black mode the liquid cr

Features (Identify each feature of your invention which you believe is new).

IMPORTANT: *Information provided by this form may be used to prepare a patent application which will be signed by the inventor(s). Inventors should take great care in accurately completing is form and in providing full information concerning prior art. False statements or concealment in obtaining a patent will subject applicant to fine and/or imprisonment (18 USC 1001) and may opardize the validity of the patent.*

WITNESSES: The two witnesses whose signature appear below have read and understand this entire invention disclosure;
Signature of Witness Date [redacted]
Signature of Witness Date [redacted]

DISCLOSURE SUBMITTED BY
Inventor's Signature Date [redacted]
Inventor's Signature Margaret Manny Date [redacted]
Inventor's Signature Date [redacted]
Inventor's Signature Date [redacted]
Inventor's Signature Date [redacted]
Inventor's Signature Date [redacted]

S/N. 08/999,663

IBM Confidential

Invention Disclosure- Additional Disclosure Page

e Each Page Must Be Signed and Dated by Every Inventor and Properly Witnessed.

tach 3 copies of any separate sketches and diagrams)

For IPLaw Use only	Disclosure Number [redacted]

cription of Invention

ystal cell thickness must be precisely controlled. (iv) If large numbers of mirrors are to be fabricated in a single array, a lithography must be developed which enables the precise fabrication of millions of mirrors over areas larger than the exposure field of step and repeat lithography tools.

The Invention

Figure one shows an embodiment of this invention. The function of the several structures and the processes used to fabricate them are: (1) A silicon wafer on which CMOS (or other forms of circuits) circuits have been fabricated and on which a passivating insulating layer has been fabricated is the starting point. (2) If needed an additional insulating layer is deposited so that it is possible to polish (chem-mech polish) the wafer flat and smooth and achieve a planarized surface. The insulating layer is for example SiO2. (3) The surface is planarized using chem-mech polishing so that either the M1 metallurgy is exposed at its highest point or so that only a thin layer of oxide (about 1000A) covers M1 at its highest point. (4) If M1 is exposed, a thin oxide layer is deposited (about 1000 A). (5) Using a lift-off or etch process a thin layer of light reflecting and absorbing material is deposited and patterned. An example of thin reflecting and absorbing material would be Cr metal followed by CrO deposited by sputtering. The total thickness would be about 1000A. The pattern is a uniform layer except for holes in the barrier to allow studs to make contact to the M1 layer below. (6) An additional layer of SiO2 is deposited or grown (possibly in two layers to eliminate pin holes). The thickness is about 2500 A. (7) Stud holes are patterned and opened in the oxide down to the M1 layer at the positions of the holes in the barrier layer. (8) These holes are filled with a flash (about 250 A) of titanium followed by several thousand angstroms of tungsten to fill the stud holes.. (9) Using the Damascene process the surface is polished down to the studs exposing them and removing all metal from the surrounding area. (10) Using a lift-off or etch process a highly reflecting metal is deposited and patterned to form the mirrors. The metal may be Al or Ag for highest reflectivity. (11) The patterning of the metal mirrors is a critical step since the eye is so sensitive to sharp edges in a pattern. Since a large array (with, say, 4 million individual mirrors on a pitch of 15 microns) is larger than the exposure field of any step and repeat lithography tool, stitching between fields with no visible discontinuity is required. Using careful alignment and a GCA stepper, we have shown that stitching alignments of about 0.1 micron can be achieved. This should be adequate for this purpose. This method also enables a gap between mirrors of one micron to be maintained. This is important to maintain a high aperture ratio. (12) An etch stop layer of 500 angstroms of Si3N4 is deposited followed by approximately 2 microns (ie the required liquid crystal cell gap thickness) of SiO2. These materials are deposited at low temperature to avoid roughen ing the mirrors. (13) A photolithography step is used with wet etching (wet

IMPORTANT: *Information provided by this form may be used to prepare a patent application which will be signed by the inventor(s). Inventors should take g* [redacted] *re in accurately completing is form and in providing full information concerning prior art. False statements or concealment in obtaining a patent will subject applicant to fine and/or imprison* *18 USC 1001) and may eopardize the validity of the patent.*

WITNESSES: The two witnesses whose signature appear below have read and understand this entire invention disclosure:

DISCLOSURE SUBMITTED BY

Signature of Witness	Date	Inventor's Signature	Date	Inventor's Signature	Date
John Hummel	[redacted]		[redacted]	Margare	[redacted]
		Frank	[redacted]		[redacted]
Cyril Cabral	[redacted]	R. L.	[redacted]	James M. E	[redacted]

S.N. 08/999,663

IBM Confidential

Invention Disclosure- Additional Disclosure Page

Page 3 of 4

For IPLaw Use only	Disclosure Number
	[redacted]

e: Each Page Must Be Signed and Dated by Every Inventor and Properly Witnessed.

tach 3 copies of any separate sketches and diagrams)

scription of Invention

etch can be glycerated BHF) and /or reactive ion etching, stopping on the etch stop layer. The photoresist layer is removed and a standard LC cell fabrication process is followed.

The resulting structure then is highly reflecting, high aperture ratio, highly planarized, provides an effective optical barrier for the circuits below, and has a precisely controlled LC cell gap thickness. A uniform aperture ratio of about 85 % is possible with a 15 micron pitch. Such an aperture ratio degrades significantly if the one micron gaps between mirrors cannot be maintained. The planarization of the surface should be possible to +/- 500A, effectively increasing the optical contrast and through-put. The reflectivity of Al is about 92 % and that of Ag is 98 % in the visible giving high optical through-put and contrast. The Cr/CrO optical barrier can be designed to have visible reflectivity between 10 and 25 %. The low reflectivity of this layer enhances the contrast ratio. The barrier prevents light from reaching the circuits below in two ways. First, through multiple reflections between the barrier and the bottom side of the mirror, the light can in principle leak down to the circuits. However, since the barrier layer is absorbing the light is attenuated with each reflection. For the small angles of incidence of the input light there will be a very large number of reflections effectively absorbing essentially all of the light. As a worst case estimate, we calculate that the input light must be attenuated by a factor of 100 000. This large factor is achieved with just five reflections if the reflection coefficient is 10 %. In practice a much larger number of reflections occur. For wavelengths of light in the oxide greater than twice the oxide thickness the barrier-oxide-mirror acts as waveguide beyond cut-off. Thus for n = 1.5 and the oxide thickness of 2500 A all wavelengths (in air) greater than 7500 A will not propagate and are very strongly attenuated. For some circuits the capacitance between the barrier and the mirrors has to be limited. This may place a practical limit on how thin the oxide can be made.

Fabrication of the spacer on the Si has significant advantages in that the spacers can be precisely aligned relative to the mirrors and the height can be controlled with a high degree of accuracy. This latter is important in order to controll the magnitude of the electrooptic effect of the cell so as to achieve a truly black state for the display at all wavelengths of light.

The Claim

What is claimed here is : (1) A light valve structure which has been fabricated directly on a Si wafer. The structure incorporates the control electronics and has been planarized. (2) A light barrier structure which effectively prevents incident light from reaching the underlying Si circuits. (3) A process and method to fabricate a large array of precisely defined highly reflecting mirrors. (4) A liquid crystal cell spacer technology consisting of SiO2 spacers which are fabricated on the light valve structure and which provide a precisely controlled cell gap thickness.

IMPORTANT: *Information provided by this form may be used to prepare a patent application which will be signed by the inventor(s). Inventors should take great care in accurately completing this form and in providing full information concerning prior art. False statements or concealment in obtaining a patent will subject applicant to fine and/or imprisonment (18 USC 1001) and may jeopardize the validity of the patent.*

WITNESSES: The two witnesses whose signature appear below have read and understand this entire invention disclosure:		DISCLOSURE SUBMITTED BY			
Signature of Witness	Date	Inventor's Signature	Date	Inventor's Signature	Date
	[redacted]		[redacted]	[redacted]	[redacted]
		Inventor's Signature	[redacted]	Inventor's Signature	[redacted]
Signature of Witness Cyril Cabral Jr.	Date [redacted]	Inventor's Signature	[redacted]	Inventor's Signature	[redacted]
		Inventor's Signature		Inventor's Signature	

S.N. 08/999,663

IBM Confidential

Invention Disclosure- Additional Disclosure Pag

Page 4 of 4

e: Each Page Must Be Signed and Dated by Every Inventor and Properly Witnessed.

tach 3 copies of any separate sketches and diagrams)

For IPLaw Use only	Disclosure Number [redacted]

scription of Invention

Implementation

Structures have been fabricated to demonstrate the efficacy of the lithography method described above. Additional experiments and evaluations are in progress to demonstrate and quantitatively evaluate the rest of the structure and process steps described above.

Potential Use

This invention is of potential interest to any company interested in projection displays of any sort. These include projection data monitors (ie Kopin, Tex. Instr., Mitsubishi, and others), projection Television (ie. Philips, Thompson, Projectavision, Hitachi, Toshiba, Sharp, Tex. Instr.,...), conference room projectors (ie Sharp, Philips, Hughes, Greyhawk, GE,Barco,...), retinal projectors (ie Virtual Vision,...). This invention may also find use a spatial light modulator in optical interconnect and optical computing. It may also be used in other applications requiring the direction of light, eg laser printing. The advantages of the present invention over other structures and fabrication methods include optical through-put, contrast and the ability to make large arrays with existing lithography tools. Other methods do not do these as well. A potential competitor to the present invention is the Texas Instruments digital mirror device which is based on a different principal. That device is proprietary to TI and its performance is not fully known by us.

References

(1) Lueder, SID 93,pg 287.

(2) Glueck et al. SID 92, pg 277.

(3) Shikama et al, SID '93, pg 295.

(4)Glueck et al, SID 93, pg 299.

IMPORTANT: *Information provided by this form may be used to prepare a patent application which will be signed by the inventor(s). Inventors should take [redacted] in accurately completing h form and in providing full information concerning prior art. False statements or concealment in obtaining a patent will subject applicant to fine and/or imprison[redacted] (18 USC 1001) and may jeopardize the validity of the patent.*

WITNESSES: The two witnesses whose signatures appear below have read and understand this entire invention disclosure:

Signature of Witness — Date [redacted]

Signature of Witness Cyril Cabral Jr. — Date [redacted]

DISCLOSURE SUBMITTED BY

Inventor's Signature — Date [redacted]

Inventor's Signature — Date [redacted]

Inventor's Signature — Date [redacted]

Inventor's Signature — Date [redacted]

Inventor's Signature — Date [redacted]

Inventor's Signature — Date [redacted]

S.N. 08/999,663

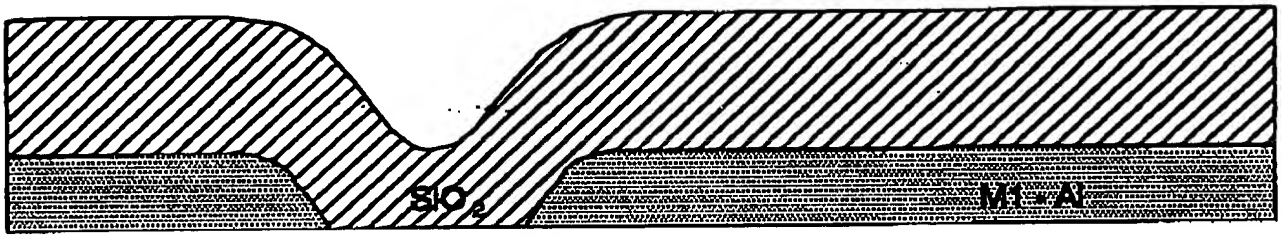
[redacted]

[redacted]

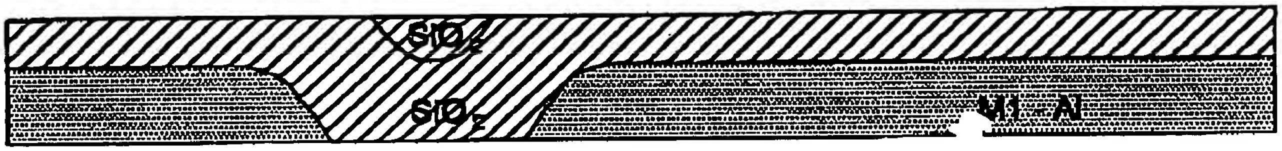
[redacted]

Fig. 1

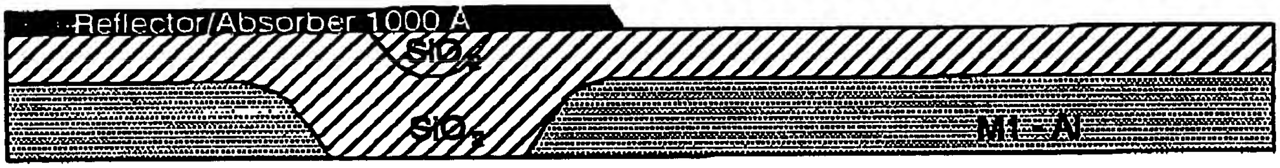
1. Semiconductor wafer w/control electronics.



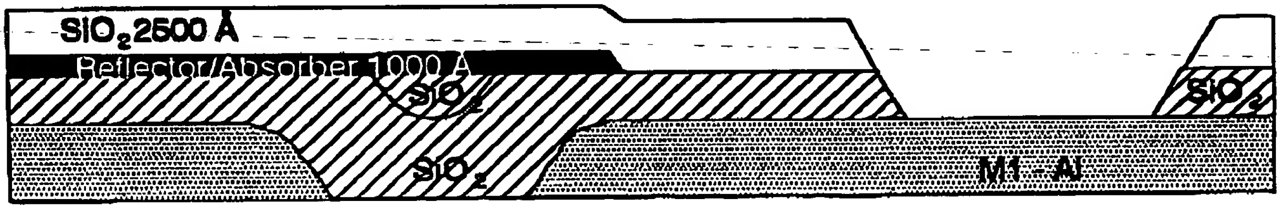
2. Deposit more SiO$_2$ and Chemical-mechanical polish



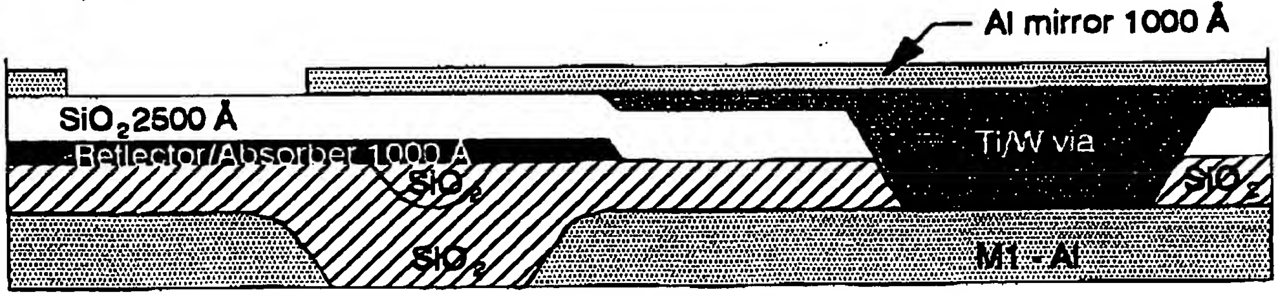
3. Deposit and pattern Reflector/Absorber layer



4. Deposit SiO$_2$, pattern via.



4. Deposit Ti/W, CMP, pattern Al mirror.



IBM Confidential

S.N. 08/999,663

[redacted]

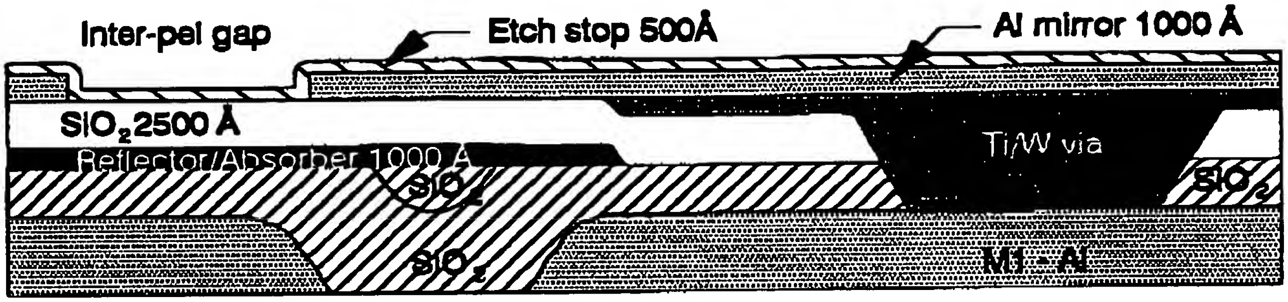
[redacted]

[redacted]

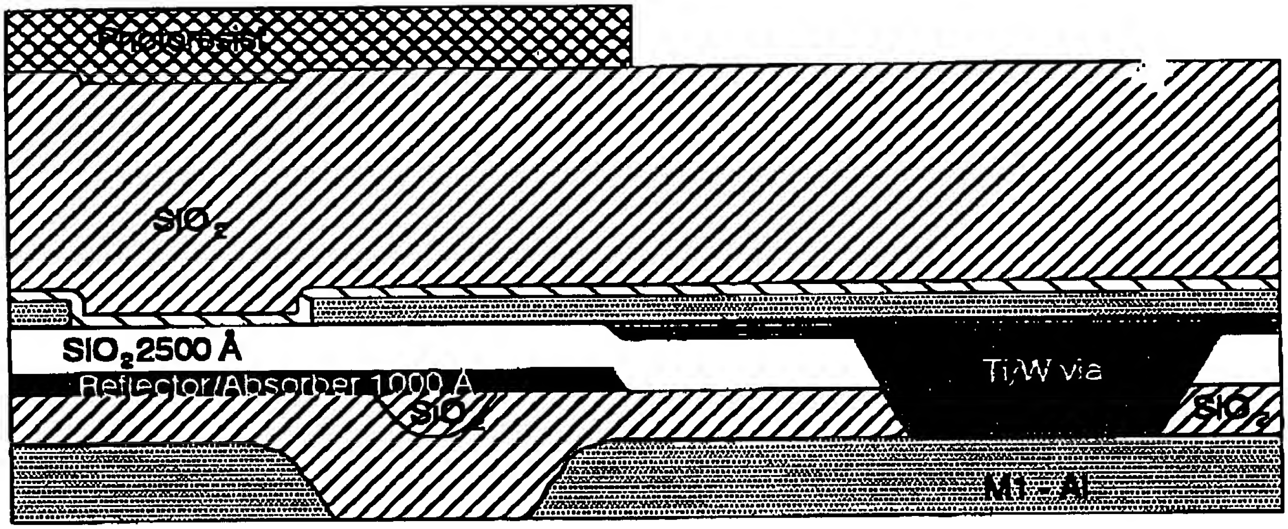
[redacted]

[redacted]

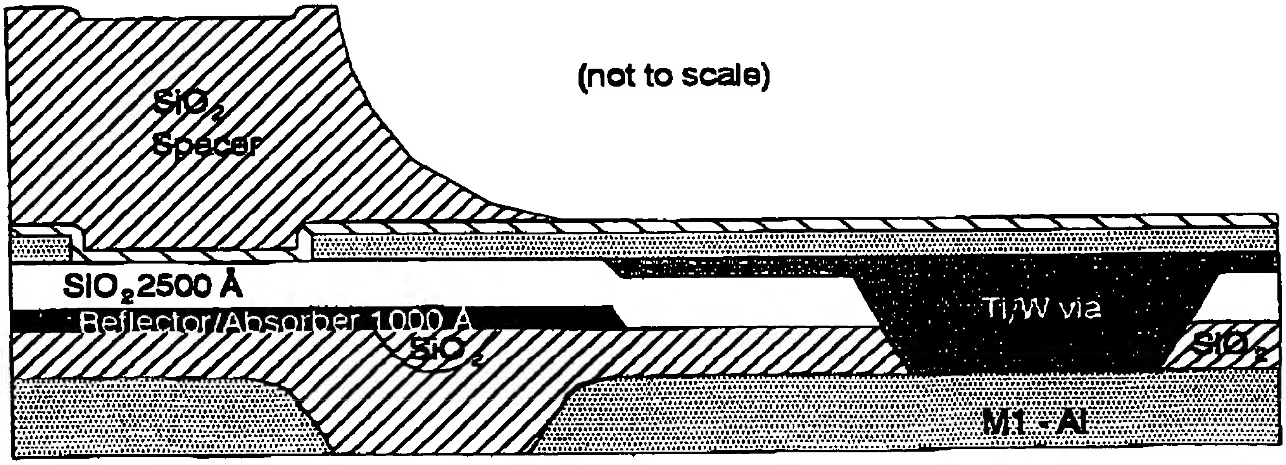
6. Deposit Etch stop on mirrors.



7. Deposit 2 μm SiO$_2$ and P.R./expose/develop.



8. Etch SiO$_2$ in Glycerated buffered HF, ash P.R..



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

E. Colgan et al.

Serial No.: 08/999,663

Filed: December 18, 1997

Date: February 1, 2000

Group Art Unit: 2871

Examiner: J. Dudek

Docket No.: YO994-065XX

For: A REFLECTIVE SPATIAL LIGHT MODULATOR ARRAY

Assistant Commissioner for Patents
Washington, D.C. 20231

CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that this paper is being facsimile transmitted under Rule 37 CFR 1.61(d) to the U.S. Patent and Trademark Office to on the date shown above.

Daniel P. Morris
Reg. No. 32,053

FAX COPY RECEIVED
APR 05 2000
TECHNOLOGY CENTER 2800

LETTER

Sir:

Enclosed is a signed Affidavit Under 37 CFR 1.131 corresponding to the unsigned Declaration submitted on January 24, 2000.

Respectfully submitted,

Daniel P. Morris
Reg. No. 32,053

IBM CORPORATION
Intellectual Property Law Dept.
P.O. Box 218
Yorktown Heights, N.Y. 10598
(914) 945-3217

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

E. Colgan et al.

Serial No. 08/999,663

Filed: December 18, 1997

Date: January 24, 2000

Group Art Unit: 2871

Examiner, J. Dudek

Docket No.: YO994-065XX

#12 Decl.
Marsha
4/10/00

For: A REFLECTIVE SPATIAL LIGHT MODULATOR ARRAY

The Commissioner of Patents and Trademarks
Washington, D.C. 20231

I hereby certify that this paper is being facsimile transmitted under Rule CFR 1.61(d) to the U.S. Patent and Trademark Office on the date shown above.

Daniel P. Morris
Reg. No. 32,053

DECLARATION UNDER 37 CFR 1.131

We, Evan G. Colgan, James M.E. Harper and James L. Speidell declares as follows:

We are co-inventors of the invention of the subject matter of the above-identified patent application. As evidenced by the attached copy of our invention disclosure we conceived and reduced the invention to practice prior to October 3, 1993 the filing date of US patent 5,461,501 to Sato et al. The attached invention disclosure was signed by us and be two witnesses and bears a time stamp of the IBM Yorktown Intellectual property Law Department prior to October 3, 1993.

By:__________________________

Evan G. Colgan,

By:__________________________

James M.E. Harper

By:__________________________
James L. Speidell

FAX COPY RECEIVED
APR 05 2000
TECHNOLOGY CENTER 2800

IBM Confidential

Page 1 of 4

IBM Invention Disclosure

12:58

FULL NAME(S) OF INVENTOR(S)	USERID/NODE	EMP. SER.	DIV/DEPT	BLDG/ZIP	LOCATION	TEL. NUM.
van Colgan 331469	862-29/ YKTVMV 4772	In NP	RES/ 743	LGA/COLGA	Yorktown	945-2909
ames M. Harper 129353	862-16/ YKTVMV 4073	In YP	RES/ 742	ARP/HARPER	Yorktown	945-1663
rank Kaufman 350004	862-32/ YKTVMV 4120	In NP	RES/ 743	/FBK	Yorktown	945-3208
argaret P. Manny 671700	862-12/ YKTVMV 4180	In YP	RES/ 748	/MANNY	Yorktown	945-1273
obert L. Melcher 763725	862-41/ YKTVMV 4003	In YP	RES/ 450	/MELCHER	Yorktown	945-4129
ames L. Speidell 592061	862-18/ YKTVMV 5001	In YP	RES/ 414	/SPEIDEL	Yorktown	945-1862

FOR USE BY IPLaw
DISCLOSURE NO. [redacted]

PATENT ATTY. RMT

EVALUATOR PPR

WHERE & WHEN RECEIVED (Time Stamp)
[redacted]
IBM YORKTOWN

TITLE OF INVENTION *(Short & Descriptive)*

Planarized Structure and Process for Reflective Light-Valve Array

PROBLEM SOLVED BY THIS INVENTION *(Summary)*

A planarized structure and process to fabricate it are described. The structure begins with a silicon wafer on which CMOS circuits have been fabricated. The wafer is then planarized using a chem-mech polish. An optical barrier is fabricated to prevent light from interacting with the underlying CMOS circuits. A stud is fabricated to make electrical contact between the CMOS circuits and individual mirrors which are to be fabricated on the wafer electrically isolated from the optical barrier an d each other. A spacer is fabricated to support the glass cover plate. A procedure is described for using a step and repeat lithographic tool to expose with geometric precision millions of individual mirrors over an area larger than the exposure field of the step and repeat tool.

ACKGROUND INFORMATION

) To what ☐ IBM Project, ☐ Proposal, ☐ or Product, ☐ or government contract is this invention related? Projection Display
) Related and background publications: None cited
) Keywords for database search for related work: Projection Display, Spatial Light Modulator, Light-Valve
) Critical Dates:
) Suggested Evaluator: DEPP HORN

VENTOR ON INTERNATIONAL ASSIGNMENT. Is any inventor of this disclosure in this country on assignment from another country?
]YES, ☑ NO. If "Yes", see instruction #5.

ESCRIPTION OF INVENTION - Provide a description *(including sketches and diagrams as required)*. On systems disclosures list significant functions and show where each is accomplished. rogramming disclosures need show only a flowchart and describe what your invention does at the level of the invention.

The Problem

Light-valve arrays are used in projection displays, optical interconnect, optical computing, and other applications in which light is to be directed in specific directions based on a prescribed function and/or pattern. (We use light-valve array and spatial light modulator synonymously). Four of the factors which affect the performance of the light-valve-array are: (i) Optical through-put. This is enhanced by using a reflective array with high aperture ratio and highly reflecting mirrors. High aperture ratio demands that the mirrors are individually large compared to the gaps between them: this requires precise fabrication.High reflectivity requires using a highly reflective metal such as Al or Ag, and fabricating it on a smooth and flat surface. (ii) Light must be kept from interacting with the underlying CMOS circuits; thus an optical barrier must be fabricated preventing the incident light from reaching the CMOS circuits. (iii) If used in the normally black mode the liquid cr

Features (Identify each feature of your invention which you believe is new).

IMPORTANT: *Information provided by this form may be used to prepare a patent application which will be signed by the inventor(s). Inventors should take great care in accurately completing this form and in providing full information concerning prior art. False statements or concealment in obtaining a patent will subject applicant to fine and/or imprisonment (18 USC 1001) and may jeopardize the validity of the patent*

WITNESSES: The two witnesses whose signature appear below have read and understand this entire invention disclosure;

Signature of Witness	Date
John Hummel	[redacted]
	[redacted]

DISCLOSURE SUBMITTED BY

Inventor's Signature	Date	Inventor's Signature	Date
Evan Colgan	[redacted]	Margaret Manny	[redacted]
Frank Kaufman	[redacted]		[redacted]
L.L. Speidell	[redacted]	Tommy M. Ettinger	[redacted]

IBM Confidential

Invention Disclosure- Additional Disclosure Page

Page 2 of 4

te: *Each Page Must Be Signed and Dated by Every Inventor and Properly Witnessed.*

For IPLaw Use only	Disclosure Number
	[redacted]

ttach 3 copies of any separate sketches and diagrams)

scription of Invention

ystal cell thickness must be precisely controlled. (iv) If large numbers of mirrors are to be fabricated in a single array, a lithography must be developed which enables the precise fabrication of millions of mirrors over areas larger than the exposure field of step and repeat lithography tools.

The Invention

Figure one shows an embodiment of this invention. The function of the several structures and the processes used to fabricat them are: (1) A silicon wafer on which CMOS (or other forms of circuits) circuits have been fabricated and on which a passivating insulating layer has been fabricated is the starting point. (2) If needed an additional insulating layer is deposited so that it is possible to polish (chem-mech polish) the wafer flat and smooth and achieve a planarized surface. The insulating layer is for example SiO2. (3) The surface is planarized using chem-mech polishing so that either the M1 metallurgy is exposed at its highest point or so that only a thin layer of oxide (about 1000A) covers M1 at its highest point. (4) If M1 is exposed, a thin oxide layer is deposited (about 1000 A). (5) Using a lift-off or etch process a thin layer of light reflecting and absorbing material is deposited and patterned. An example of thin reflecting and absorbing material would be Cr metal followed by CrO deposited by sputtering. The total thickness would be about 1000A. The pattern is a uniform layer except for holes in the barrier to allow studs to make contact to the M1 layer below. (6) An additional layer of SiO2 is deposited or grown (possibly in two layers to eliminate pin holes). The thickness is about 2500 A. (7) Stud holes are patterned and opened in the oxide down to the M1 layer at the positions of the holes in the barrier layer. (8) These holes are filled with a flash (about 250 A) of titanium followed by several thousand angstroms of tungsten to fill the stud holes.. (9) Using the Damascene process the surface is polished down to the studs exposing them and removing all metal from the surrounding area. (10) Using a lift-off or etch process a highly reflecting metal is deposited and patterned to form the mirrors. The metal may be Al or Ag for highest reflectivity. (11) The patterning of the metal mirrors is a critical step since the eye is so sensitive to sharp edges in a pattern. Since a large array (with, say, 4 million individual mirrors on a pitch of 15 microns) is larger than the exposure field of any step and repeat lithography tool, stitching between fields with no visible discontinuity is required. Using careful alignment and a GCA stepper, we have shown that stitching alignments of about 0.1 micron can be achieved. This should be adequate for this purpose. This method also enables a gap between mirrors of one micron to be maintained. This is important to maintain a high aperture ratio. (12) An etch stop layer of 500 angstroms of Si3N4 is deposited followed by approximately 2 microns (ie the required liquid crystal cell gap thickness) of SiO2. These materials are deposited at low temperature to avoid roughen ing the mirrors. (13) A photolithography step is used with wet etching (wet

IMPORTANT: *Information provided by this form may be used to prepare a patent application which will be signed by the inventor(s). Inventors should take g* [redacted] *e in accurately completing this form and in providing full information concerning prior art. False statements or concealment in obtaining a patent will subject applicant to fine and/or imprison* [redacted] *(18 USC 1001) and may jeopardize the validity of the patent.*

WITNESSES: The two witnesses whose signature appear below have read and understand this entire invention disclosure;		DISCLOSURE SUBMITTED BY			
Signature of Witness	Date	Inventor's Signature	Date	Inventor's Signature	Date
	[redacted]		[redacted]	[redacted]	[redacted]
		Inventor's Signature		Inventor's Signature	Date
			[redacted]		[redacted]
Signature of Witness	Date	Inventor's Signature	Date	Inventor's Signature	Date
	[redacted]		[redacted]	James M.E	[redacted]
		Inventor's Signature	Date	Inventor's Signature	Date

IBM Confidential

Invention Disclosure- Additional Discl sur Page

Page 3 f 4

te: Each Page Must Be Signed and Dated by Every Inventor and Properly Witnessed.

ttach 3 copies of any separate sketches and diagrams)

For IPLaw Use only	Disclosure Number [redacted]

scription of Invention

etch can be glycerated BHF) and /or reactive ion etching, stopping on the etch stop layer. The photoresist layer is removed and a standard LC cell fabrication process is followed.

The resulting structure then is highly reflecting, high aperture ratio, highly planarized, provides an effective optical barrier for the circuits below, and has a precisely controlled LC cell gap thickness. A uniform aperture ratio of about 85 % is possible with a 15 micron pitch. Such an aperture ratio degrades significantly if the one micron gaps between mirrors cannot be maintained. The planarization of the surface should be possible to +/- 500A, effectively increasing the optical contrast and through-put. The reflectivity of Al is about 92 % and that of Ag is 98 % in the visible giving high optical through-put and contrast. The Cr/CrO optical barrier can be designed to have visible reflectivity between 10 and 25 %. The low reflectivity of this layer enhances the contrast ratio. The barrier prevents light from reaching the circuits below in two ways. First, through multiple reflections between the barrier and the bottom side of the mirror, the light can in principle leak down to the circuits. However, since the barrier layer is absorbing the light is attenuated with each reflection. For the small angles of incidence of the input light there will be a very large number of reflections effectively absorbing essentially all of the light. As a worst case estimate, we calculate that the input light must be attenuated by a factor of 100 000. This large factor is achieved with just five reflections if the reflection coefficient is 10 %. In practice a much larger number of reflections occur. For wavelengths of light in the oxide greater than twice the oxide thickness the barrier-oxide-mirror acts as waveguide beyond cut-off. Thus for n = 1.5 and the oxide thickness of 2500 A all wavelengths (in air) greater than 7500 A will not propagate and are very strongly attenuated. For some circuits the capacitance between the barrier and the mirrors has to be limited. This may place a practical limit on how thin the oxide can be made.

Fabrication of the spacer on the Si has significant advantages in that the spacers can be precisely aligned relative to the mirrors and the height can be controlled with a high degree of accuracy. This latter is important in order to controll the magnitude of the electrooptic effect of the cell so as to achieve a truly black state for the display at all wavelengths of light.

Th Claim

What is claimed here is : (1) A light valve structure which has been fabricated directly on a Si wafer. The structure incorporates the control electronics and has been planarized. (2) A light barrier structure which effectively prevents incident light from reaching the underlying Si circuits. (3) A process and method to fabricate a large array of precisely defined highly reflecting mirrors. (4) A liquid crystal cell spacer technology consisting of SiO2 spacers which are fabricated on the light valve structure and which provide a precisely controlled cell gap thickness.

IMPORTANT: *Information provided by this form may be used to prepare a patent application which will be signed by the inventor(s). Inventors should take great care in accurately completing this form and in providing full information concerning prior art. False statements or concealment in obtaining a patent will subject applicant to fine and/or imprisonment (18 USC 1001) and may jeopardize the validity of the patent*

WITNESSES: The two witnesses whose signature appear below have read and understand this entire invention disclosure;		DISCLOSURE SUBMITTED BY			
Signature of Witness	Date [redacted]	Inventor's Signature Inventor's Signature	Date [redacted]	Inventor's Signature Inventor's Signature [redacted]	Date [redacted]
Signature of Witness Cyril Cabral Jr	Date [redacted]	Inventor's Signature Inventor's Signature		Inventor's Signature Inventor's Signature	[redacted]

IBM Confidential

Invention Disclosure- Additional Disclosure Page

Page 4 of 4

For IPLaw Use only	Disclosure Number [redacted]

ote: Each Page Must Be Signed and Dated by Every Inventor and Properly Witnessed.

ttach 3 copies of any separate sketches and diagrams)

scription of Invention

Implementation

Structures have been fabricated to demonstrate the efficacy of the lithography method described above. Additional experiments and evaluations are in progress to demonstrate and quantitatively evaluate the rest of the structure and process steps described above.

Potential Use

This invention is of potential interest to any company interested in projection displays of any sort. These include projection data monitors (ie Kopin, Tex. Instr., Mitsubishi, and others), projection Television (ie. Philips, Thompson, Projectavision, Hitachi, Toshiba, Sharp, Tex. Instr.,...), conference room projectors (ie Sharp, Philips, Hughes, Greyhawk, GE,Barco,...), retinal projectors (ie Virtual Vision,...). This invention may also find use as a spatial light modulator in optical interconnect and optical computing. It may also be used in other applications requiring the direction of light, eg laser printing. The advantages of the present invention over other structures and fabrication methods include optical through-put, contrast and the ability to make large arrays with existing lithography tools. Other methods do not do these as well. A potential competitor to the present invention is the Texas Instruments digital mirror device which is based on a different principal. That device is proprietary to TI and its performance is not fully known by us.

References

(1) Lueder, SID 93,pg 287.

(2) Glueck et al. SID 92, pg 277.

(3) Shikama et al, SID '93, pg 295.

(4)Glueck et al, SID 93, pg 299.

IMPORTANT: *Information provided by this form may be used to prepare a patent application which will be signed by the inventor(s). Inventors should take gr[redacted]re in accurately completing this form and in providing full information concerning prior art. False statements or concealment in obtaining a patent will subject applicant to fine and/or imprison (18 USC 1001) and may jeopardize the validity of the patent*

WITNESSES: The two witnesses whose signature appear below have read and understand this entire invention disclosure;		DISCLOSURE SUBMITTED BY			
Signature of Witness	Date [redacted]	Inventor's Signature	Date [redacted]	Inventor's Signature	Date [redacted]
		Inventor's Signature	[redacted]	Inventor's Signature	[redacted]
Signature of Witness Cyril Cabral Jr	Date [redacted]	Inventor's Signature	[redacted]	Inventor's Signature	[redacted]
		Inventor's Signature	Date	Inventor's Signature	Date

[redacted]

[redacted]

[redacted]

Frank

James E.

[redacted]

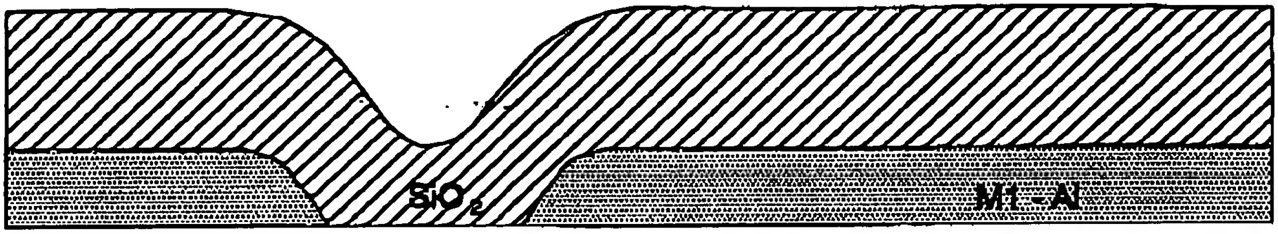
[redacted]

[redacted]

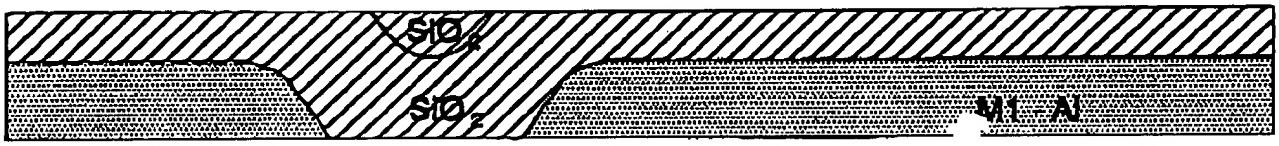
[redacted]

Fig. 1

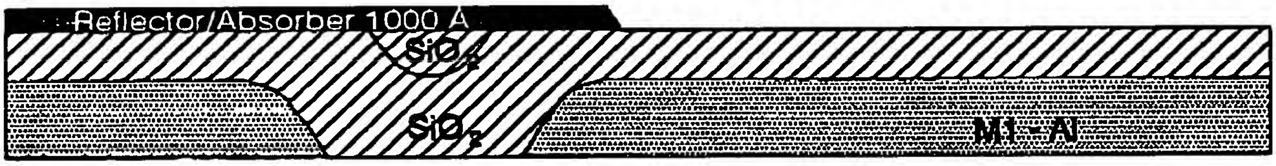
1. Semiconductor wafer w/control electronics.



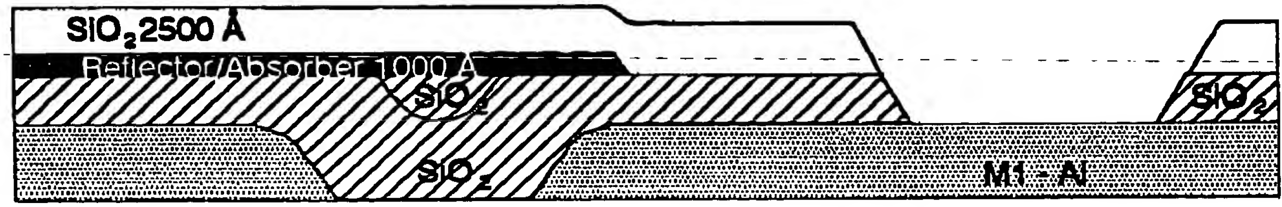
2. Deposit more SiO_2 and Chemical-mechanical polish



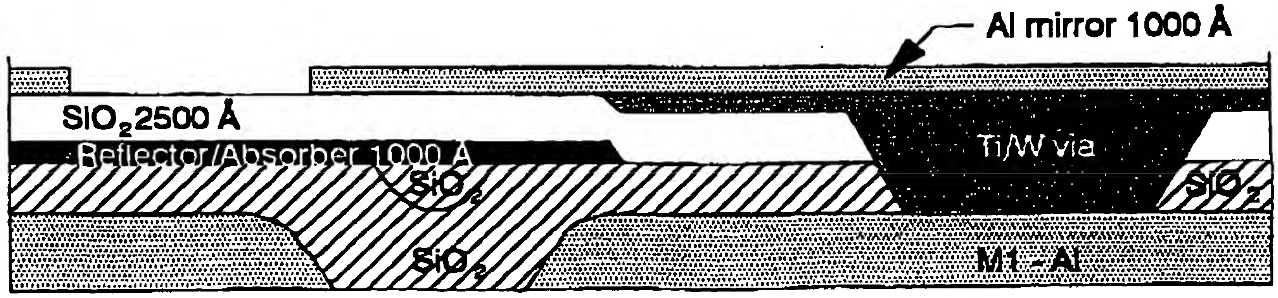
3. Deposit and pattern Reflector/Absorber layer



4. Deposit SiO_2, pattern via.



4. Deposit Ti/W, CMP, pattern Al mirror.



IBM Confidential

[redacted]

[redacted]

[redacted]

[redacted]

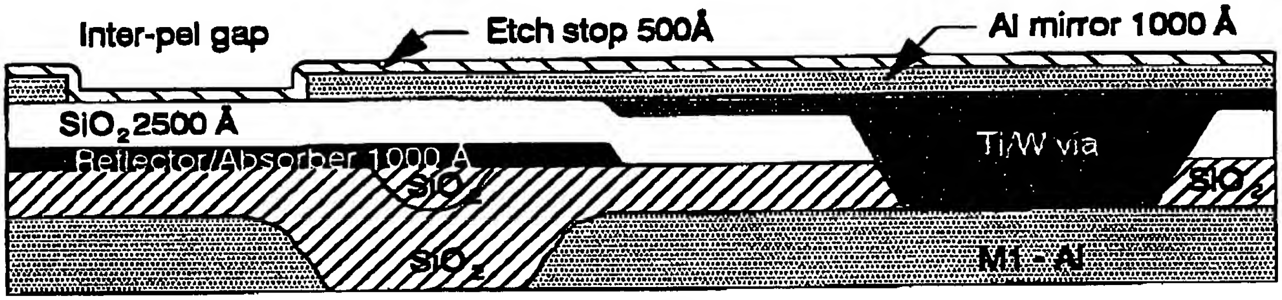
[redacted]

[redacted]

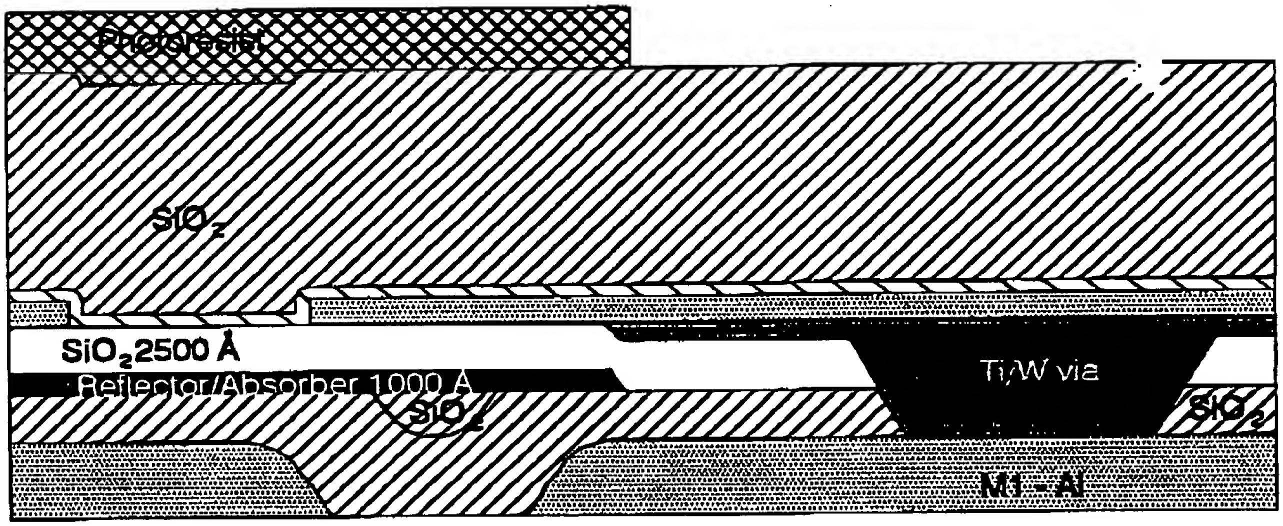
[redacted]

[redacted]

6. Deposit Etch stop on mirrors.



7. Deposit 2 μm SiO$_2$ and P.R./expose/develop.



8. Etch SiO$_2$ in Glycerated buffered HF, ash P.R..